IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently amended): A semiconductor device, comprising:

a semiconductor layer which includes a first semiconductor region of a first conductivity type, a base region of a second conductivity type formed above the first semiconductor region, and a plurality of second semiconductor regions of the first conductivity type formed on the base region;

[[a]] at least one gate electrode which is formed between the first semiconductor region and the second semiconductor regions and which is adjacent to the first semiconductor region and the second semiconductor regions, the gate electrode facing the base region via a gate insulating film;

a gate wiring which is formed on the semiconductor layer via a first insulating film and which is made of metal, the gate wiring being electrically connected to the gate electrode;

a plurality of main electrodes which are electrically connected to the plurality of second semiconductor regions, wherein the gate wiring is arranged between the main electrodes and the gate wiring is ~~not electrically connected to~~ separated from the main electrodes by a second insulating film; and

a connecting plate which is connected onto upper surfaces of the main electrodes, wherein the main electrodes are in contact with a contact region of the connecting plate, and, in an area under the contact region of the connecting plate, the highest portion of an uppermost surface of the gate wiring is not higher than the upper surfaces of the main electrodes, wherein the connecting plate is connected to a lead frame and the gate wiring is not electrically connected to the connecting plate.

Claim 2 (Withdrawn-Previously presented): The semiconductor device according to claim 1, wherein uppermost surfaces of the plurality of main electrodes are a metal.

Claim 3 (Cancelled).

Claim 4 (Currently amended): The semiconductor device according to claim 54, wherein the main electrodes are formed of a plurality of metal layers, and the third ~~second~~ insulating film extends between the plurality of metal layers.

Claim 5 (Original): The semiconductor device according to claim 1, wherein the plurality of main electrodes are formed apart from the gate wiring with a gap therebetween.

Claims 6-44 (Canceled)

Claim 45 (Previously presented): The semiconductor device according to claim 1, wherein the main electrodes comprise a first main electrode layer and a second main electrode layer which is formed on the first main electrode layer.

Claim 46 (Currently amended): The semiconductor device according to claim 45, wherein the second main electrode ~~is formed on the second~~ is electrically connected to the first main electrode via an opening formed in a fourth insulating film which is formed on the first main electrode.

Claim 47 (Previously presented): The semiconductor device according to claim 45, wherein the second main electrode is thicker than the first main electrode layer.

Claims 48-51 (Canceled)

Claim 52 (Previously presented): The semiconductor device according to claim 1, wherein the upper surfaces of the main electrodes are higher than the highest portion of an uppermost surface of the gate wiring.

Claim 53 (Previously presented): The semiconductor device according to claim 1, wherein the connecting plate is directly connected onto the upper surfaces of the main electrodes.

Claim 54 (Currently amended): The semiconductor device according to claim 1, wherein a ~~second~~ third insulating film is formed on the gate wiring so as to insulate the gate wiring from the connecting plate.

Claim 55 (Previously presented): The semiconductor device according to claim 1, wherein the main electrodes comprises first electrodes and second electrodes which are formed above the first electrodes,

upper surfaces of the second electrodes are directly connected to the connecting plate, and

the highest portion of an uppermost surface of the gate wiring is not higher than the upper surfaces of the second electrodes.

Claim 56 (Currently amended): A semiconductor device, comprising:

a first semiconductor region of a first conductive type;

a second semiconductor region of a second conductive type, the second semiconductor region being formed above the first semiconductor region;

a third semiconductor region of the first conductive type, the third semiconductor region being formed above the second semiconductor region;

[[a]] at least one gate electrode which is formed between the first semiconductor region and the third semiconductor region and which is adjacent to the first semiconductor region and the third semiconductor region, the gate electrode facing the second semiconductor region via a gate insulating film;

a first main electrode which is divided into a plurality of first main electrode units, the first main electrode units being electrically connected to the second semiconductor region and the third semiconductor region;

a metal gate wiring which is electrically connected to the gate electrode and which is arranged between the first main electrode units, wherein the metal gate wiring is separated from the first main electrode by a first insulating film;

a lead frame; and

a connecting plate which is connected to the first main electrode units and the lead frame by ultrasonic bonding so as to electrically connect the first main electrode units to the lead frame, the connecting plate being in the form of a plate, wherein the first main electrode units are connected to the connecting plate by the ultrasonic bonding such that the connecting plate covers at least a portion of the first main electrode units between which the metal gate wiring is arranged, and wherein the metal gate wiring ~~does~~ is not electrically ~~connect~~ connected to the connecting plate which is over the metal gate wiring.

Claim 57 (Previously presented): The semiconductor device according to claim 56, wherein the highest portion of an uppermost surface of the metal gate wiring is lower than a bottom surface of a portion of the connecting plate which is over the metal gate wiring.

Claim 58 (Previously presented): The semiconductor device according to claim 57, wherein the highest portion of the uppermost surface of the metal gate wiring is lower than an upper surfaces of the first main electrode units.

Claim 59 (Currently amended): The semiconductor device according to claim 57, wherein ~~an~~ a second insulating film is formed between the metal gate wiring and the connecting plate.

Claim 60 (Previously presented): The semiconductor device according to claim 57, further comprising a fourth semiconductor region of the second conductive type, the fourth semiconductor region being formed on a side of the first semiconductor region which is opposite to the second semiconductor region.

Claim 61 (Previously presented): The semiconductor device according to claim 57, further comprising a second main electrode which is formed on a side of the first semiconductor region which is opposite to the second semiconductor region, the second main electrode being electrically connected to the first semiconductor region.

Claim 62 (Previously presented): The semiconductor device according to claim 60, further comprising a second main electrode which is formed on a side of the fourth

semiconductor region which is opposite to the first semiconductor region, the second main electrode being electrically connected to the fourth semiconductor region.

Claim 63 (Previously presented): The semiconductor device according to claim 57, wherein the gate electrode is formed in a trench with the gate insulating film, wherein the trench passes through the second semiconductor region so as to reach the first semiconductor region.

Claim 64 (Previously presented): The semiconductor device according to claim 57, wherein the connecting plate is made of aluminum.

Claim 65 (Previously presented): The semiconductor device according to claim 57, wherein the connecting plate covers a major part of the first main electrode units.

Claim 66 (Previously presented): The semiconductor device according to claim 57, wherein a gap is formed between the first main electrode units and the metal gate wiring.

Claim 67 (Previously presented): The semiconductor device according to claim 57, wherein the connecting plate is directly connected to the first main electrode units and the lead frame.

Claim 68 (Previously presented): The semiconductor device according to claim 61, wherein the semiconductor device is a vertical MOSFET.

Claim 69 (Previously presented): The semiconductor device according to claim 62, wherein the semiconductor device is an IGBT.

Claim 70 (New): The semiconductor device according to claim 1, wherein a plurality of gate electrodes are provided and the main electrodes are formed above the plurality of gate electrodes with a gap therebetween, and the gate wiring is arranged in the gap so that the gate wiring is not in contact with the connecting plate and the gate wiring is located between the plurality of gate electrodes, and

the second semiconductor regions are formed on a first side of the plurality of gate electrodes and the second semiconductor regions are not formed on a second side of the plurality of gate electrodes, the second side of the plurality of gate electrodes is an inner side in which the gate wiring is located.

Claim 71 (New): The semiconductor device according to claim 56, wherein a plurality of gate electrodes are provided and the main electrodes are formed above the plurality of gate electrodes with a gap therebetween, and the gate wiring is arranged in the gap so that the gate wiring is not in contact with the connecting plate and the gate wiring is located between the plurality of gate electrodes, and

the second semiconductor regions are formed on a first side of the plurality of gate electrodes and the second semiconductor regions are not formed on a second side of the plurality of gate electrodes, the second side of the plurality of gate electrodes is an inner side in which the gate wiring is located.